REMARKS

Favorable reconsideration of this application is currently constituted as respectfully requested.

Claims 1, 13, 19 and 25 have been amended. Claims 1-7, 13-23 and 25 remain active in this application, with Claims 8-12 having previously been withdrawn from consideration.

Previously presented Claims 1, 5, 7, 13, 18 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Zimmerman*, U.S. Patent No. 5,172,213 in view of *Casto*, U.S. Patent No. 5,172,214.

Claims 2-4, 6, 14-17 and 20-25 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Zimmerman, supra*, and *Casto, supra* in view of *Aono et al.*, U.S. Patent No. 5,521,429. Applicants respectfully traverse the rejections of record.

A clean copy of pending claims is attached hereto as **Appendix A** for the Examiner's convenience. A marked-up copy of the claims as amended herein is attached hereto as **Appendix B**.

Before discussing in detail the rejection of the claims on their merits, it is believed that a brief recapitulation of the subject matter of Applicants' invention might be useful. Applicants' invention is directed to a novel semiconductor package and packaged semiconductor in which the thermal characteristics and moisture resistant characteristics are significantly improved over prior art devices.

Specifically, Applicants' invention, as currently claimed, uses a chip paddle, which is thicker in one portion and around which a plurality of internal leads are arranged in regular intervals. These internal leads are at one portion as thick as the chip paddle in its thickest portion, so that the upper surface of the internal lead and the upper surface of the chip paddle can be approximately coplanar. The invention contains further innovations: the bottom surface of the chip paddle and the internal leads are approximately coplanar on their opposite side; the

upper surface of the internal leads and the upper surface of the chip paddle can be approximately coplanar; and the upper surface of the internal leads and an intermediate surface of the chip paddle can be approximately coplanar. However, both the chip paddle and the internal leads have etched portions so that they are thinner in an area around the central core of the chip paddle, which is normally the thickest portion of the chip paddle. This provides a locking area which allows the body to have an increased locking strength when an encapsulate is provided. It also provides that the encapsulation material minimizes the influence of moisture on the semiconductor package in the finished device. This influence of moisture is minimized by lengthening any passage through which moisture might permeate into the semiconductor chip itself.

The *Zimmerman* reference in Figures 1 and 2 by way of illustration shows a conventional lead packaging with at most a heat dissipating post placed on top of the semiconductor chip. This is quite different than the type of chip paddle called for in Applicants' invention, which supports the semiconductor chip, and which extends to the bottom of the package. Furthermore, there is nothing in the *Zimmerman* reference in any manner which teaches or suggests that the chip paddle be used in a manner, be etched in a manner, or formed in a manner as to provide a locking mechanism for the encapsulate as in Applicants' device by having, for example, a surface of the chip paddle and at least one portion of the upper, lower, or both upper and lower surfaces of the internal leads being in an approximately common plane and wherein the chip paddle is at least in one part thicker than at least a portion of the internal leads. This difference in thickness between the chip paddle and the internal leads provides for a locking by the encapsulate and also provides the aforementioned amelioration of the moisture problems of the semiconductor chip in prior art devices.

The *Casto* reference, as can be seen from Figure 1 of the *Casto* disclosure, does not teach that the thickness of the leads should be varied, nor should thickness of the chip paddle, and it is clear from a review of Figure 1 of the *Casto* reference that it is contemplated that the thickness of

the chip paddle 65 and the lead thickness 68 of the *Casto* reference be identical along their entire lengths. Accordingly, it cannot be said that there is a difference between the thicknesses of the two items and wherein the chip paddle is in at least one part thicker than at least one part of the internal leads.

The *Aono et al.* reference, although showing a difference in the thickness between the chip paddle 15 and the leads 16/12, clearly shows the opposite approach taken from Applicants' invention, where the chip paddle 15 is in fact thinner along its entire surface than the leads 16/12. Accordingly, it cannot be said that the *Aono et al.* reference teaches Applicants' invention, but rather teaches in a direction opposite that of Applicants' invention. The aforementioned problem of moisture penetration would be present in the *Aono et al.* reference in that the path by which the moisture might take is not lengthened by the *Aono et al.* reference in any manner.

In view of the foregoing difference between Applicants' invention and the prior art, as currently claimed, it is believed that Applicants' invention is patentably distinguishable from all references currently of record. Applicants', therefore, respectfully request the thorough reconsideration of this application and earnestly solicit an early notice of allowance.

Respectfully submitted,
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APPENDIX B - RE-WRITTEN CLAIMS MARKED-UP TO SHOW CHANGES AFTER RESPONSE TO OFFICE ACTION DATED OCTOBER 24, 2001:

1. (Twice Amended) A semiconductor package, comprising:

a semiconductor chip provided with a plurality of input/output pads on its upper surface;

a chip paddle adjacent a bottom surface of the semiconductor chip, said chip paddle having an upper surface;

a plurality of internal leads surrounding the chip paddle wherein the upper surface of the chip paddle and at least one portion of an upper surface of the internal leads are in approximately a common plane, and wherein the chip paddle is in at least one part thicker than at least a portion of the internal leads;

conductive wires for electrically connecting the input/output pads of the semiconductor chip to the internal leads; and

a package body comprised of encapsulation material that encapsulates the semiconductor chip, the conductive wires, the chip paddle and the internal leads, wherein the chip paddle and the internal leads are externally exposed at a bottom surface of the chip paddle and the internal leads.

13. (Twice Amended) A packaged semiconductor, comprising:

a chip paddle adapted to receive a semiconductor chip, said chip paddle having an upper surface, a lower surface, and an intermediate surface positioned between and parallel to the upper surface and the lower surface;

a plurality of internal leads surrounding the chip paddle wherein the chip paddle and the leads comprise a leadframe wherein the intermediate surface of the chip paddle and at least one portion of an upper surface of the internal leads are in approximately a common plane, and wherein the chip paddle is at least one part thicker than at least a portion of the internal leads; and

the leadframe adapted to receive a package body comprised of encapsulation material for encapsulating the chip paddle and the internal leads, wherein the chip paddle and the internal leads are externally exposed at a bottom surface of the chip paddle and the internal leads.

19. (Amended) A package for mounting a semiconductor chip, comprising:

a leadframe, the leadframe comprising;

a chip paddle wherein a surface of the chip paddle is externally exposed from the package; and

a plurality of internal leads surrounding the chip paddle, wherein a surface of each of the plurality of internal leads is externally exposed from the package;

means for receiving encapsulating material for encapsulating the leadframe;

means for locking the encapsulating means to the chip paddle;

means for providing a fluid path for the encapsulating means during encapsulation of the leadframe; and

said means for [removing fluid from the package.] locking and said means for providing a fluid path are formed from a void caused by said chip paddle being in at least one part thicker than at least a portion of the internal leads.

25. (Amended) The package as set forth in claim 21, wherein the etched portion is located inside the package body, an upper surface of the chip paddle and a lower surface of the plurality of internal leads are in approximately a common plane, [and wherein the chip paddle is thicker than the at least one of the plurality of internal leads,] the chip paddle is bonded to a bottom surface of a semiconductor chip and at least one of the plurality of internal leads has an etched part at an end facing the chip paddle.